Three-Phase Multilevel PFC Rectifier Based on Multistate Switching Cells

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***Abstract*—This paper presents a three-phase multilevel power factor correction (PFC) rectifier employing multistate switching cells. A generalized converter structure is presented based on the connection of switching networks of Vienna-type rectifier topologies through multiinterphase transformers (MIPTs). The resulting rectifier presents the intrinsic benefits to the employed building blocks and the ones added by a modular construction that enables the reduction of passive components and overall losses. The operation of the PFC rectifier is described, including appropriate modulation and control strategies. Design guidelines for the magnetic components are derived for the MIPTs, boost inductors, and power semiconductor devices. Finally, a lab prototype is used to present experimental results. This prototype is rated at 7.5 kW and uses a modular structure to assemble a four legs per phase rectifier. Efficiency above 98% from 40% load and IEC61000-3-2 requirements are observed.**

***Index Terms*—High efficiency, high power density, multistate switching cells, power factor correction, PWM rectifiers.**

I. Introduction

THE electric power demand increase has triggered discussions concerning the production, transmission, and distribution of electric energy in the last decades. Substantial research resources have been put into new and renewed power processing concepts, such as the use of renewable energy sources and distributed generation. At the same time, the needs for energy and the risk of shortages generated a discussion on how electric energy is spent. Low-efficiency equipment are present in both residential and industrial environments, and are responsible for a considerable amount of the demanded energy and material resources. In this sense, it is clear that energy processing efficiency and reduced raw materials usage are key factors for a sustainable society.

Unidirectional power factor correction (PFC) rectifiers play an important role in such scenario, since high-power electronic loads are effectively fed by such rectifiers due to the predominantly alternating current (ac) power distribution networks. Such converters have been widely employed to improve the power quality in high-power ac to direct current (dc) conversion systems. Various topologies were proposed [1], [2]. Especially, the three-level three-phase unidirectional rectifiers [3], [4] provide the means to achieve benefits that include [5] high power factor; control of the dc output voltage; the possibility to use lower voltage power semiconductors, e.g., 600-V MOSFETs in 400-V mains applications; robustness, since shoot through is not possible; reduced passive components due to lower noise generation; and high conversion efficiency. Another trend perceived in power electronics is the increase in the electronically processed power levels, e.g., grid applications [6], [7] and high-power variable speed drives [8]. This trend to higher processed power has been mainly driven by the evolution of power semiconductors [9]–[12]. However, the development of modular converter concepts has been also an important part in this process [13]. The typical aims in the high power are to increase reliability and reduce costs, both initial and operational. Reducing power conversion losses helps in both these objectives by lowering cooling systems requirements, and thus, high efficiency appears as a goal even under this perspective. This paper presents multistate switching cell-based multilevel PFC rectifiers (MLMSR) [14]–[21] and shows that these are a promising solution in this context. Remarkably high-efficiency rctifiers built with this type of technology were reported in [22] and [23]. MLMSRs have all the benefits of three-level three-phase unidirectional rectifiers and can be built in a modular way. Thus, very high power ratings and/or very compact implementations are possible.

This paper introduces MLMSRs as a generalized converter topology, where the switching network structure can be changed to achieve the characteristics of more basic nonmodularized three-phase three-level rectifier topologies. Different magnetic components and architectures are discussed in Section II and provide flexible ways to implement the rectifiers. A brief review of multistate switching cells and an appropriate modulation strategy are also presented in Section II to introduce the basic operation of the proposed concept. The operation of MLMSRs as PFC circuits is defined and the resulting switching voltages are derived in Section III. This section also analyzes the generation of current ripple in the boost inductors as well as in the multiinterphase transformers (MIPTs) magnetizing inductance are analyzed and defines a suitable control strategy. Section IV presents a discussion and design guidelines to the choice of switching networks. A laboratory prototype is described in Section V used to provide experimental results that verify the described operation of an MLMSR. This prototype is rated at 380 V/7.5 kW and has the characteristics of not using heatsinks, i.e., the generated heat is dissipated by forced air cooling flowing through modular printed circuit boards that physically implement the switching networks. The achieved efficiency is above 98% from 40% load and above 96% from 7%

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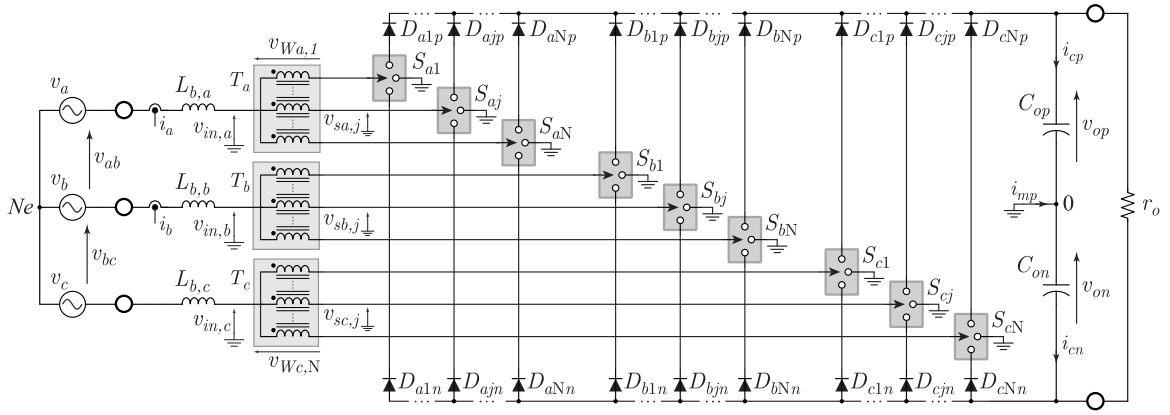

Fig. 1. General circuit structure of the multilevel multistate switching cell-based three-phase unidirectional rectifier (MLMSR).

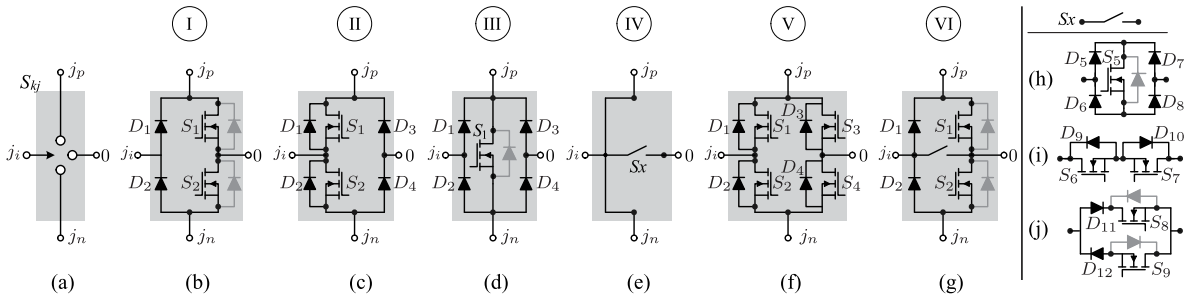

Fig. 2. SPTT switches . (a) Generic representation. (b)–(g) Practical implementation examples of the SPTT switches. (h)–(j) Bidirectional switch implementation alternatives to be employed in configurations (e) and (g).

load and IEC61000-3-2 Class A standard [24] requirements are met.

II. Three-Phase Multilevel PFC With Multistate Switching Cells

The proposed multilevel three-phase PFC rectifiers employing multistate switching cells, shown in Fig. 1, are an extension of the single-phase ones introduced in [18], [25], and [26]. However, their three-phase characteristics make them more efficient, even though more complex. This section describes the basic operation of such rectifiers driven by pulse width modulation (PWM).

The converter is fed from a three-phase three-wire ac power system. It is assumed that the grid phase voltages are balanced and defined with

$$v_k = \hat{V}_g \sin\left(\omega_g t + \phi_k\right) \tag{1}$$

where $\hat{V}_g$ and ω_g are the peak phase-voltage value and the angular frequency of the grid, respectively, and $k = a, b, c$. Thus, the phase angles ϕ_k are $\phi_a = 0$ rad, $\phi_b = -2\pi/3$ rad, and $\phi_c = +2\pi/3$ rad.

Three dc voltage levels, namely v_{op}, 0, and $v_{\rm on}$ are on the dc-link at the output side. The total dc-link voltage is

$$v_o = v_{op} + v_{\rm on}. \tag{2}$$

The MLMSR has three phases, where each rectifier phase is composed of N semiconductor legs (identified with index j, with $j = 1, 2, \ldots, N$). Three boost inductors $L_{b,k}$ interface the converter to the grid voltages. A MIPT T_k with N windings connects the respective boost inductor $L_{b,k}$ to N semiconductor legs. Each leg is composed of a single pole triple throw (SPTT) switch S_{kj}, diodes D_{kjp}, and D_{kjn}, where the subindices p and n refer to the diodes connected to the positive p and negative n dc-link terminals, respectively. These diodes are used to maintain the unidirectional nature of the converter, but can be omitted for specific analyzes, for instance to obtain control oriented models.

Various switch configurations are able to implement S_{kj}. The ones presented in Fig. 2 [3], [4], [25], [27]–[30] are well-proven examples. However, the generic representation of an SPTT in Fig. 1 is considered for the converter operation analysis described in the following. The semiconductors efforts and practical implementation issues related to the SPTT configurations are further discussed in Section IV.

The MIPTs T_k have been named differently in the literature. Cougo *et al.* [31], [32] use intercell transformers, while the first reference on this subject related to PFC rectifiers [14] uses autotransformers, and the authors in [33] and [34] use highly and close-coupled inductors, respectively. The first work to propose the association of bidirectional multilevel converter legs with this type of magnetic component [35] used the term current-sharing reactors. This study chooses to use MIPT as in [36] given

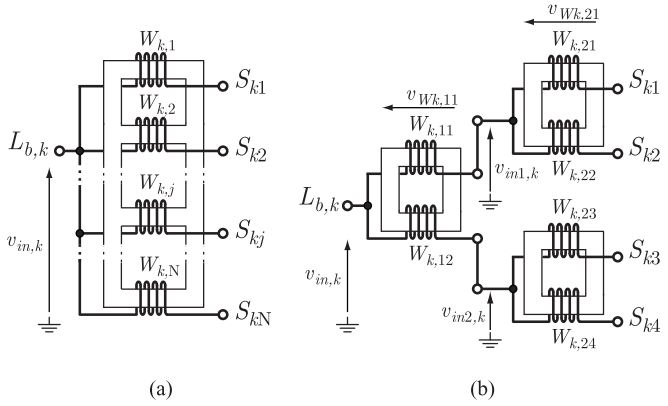

Fig. 3. (a) Basic implementation of an N-winding MIPT, where an asymmetrical N-limb core is illustrated. (b) Whiffletree alternative for a practical $N = 4$ converter implementation.

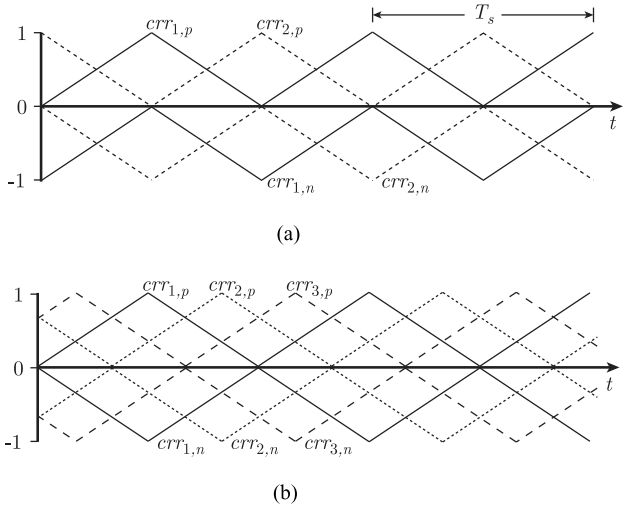

Fig. 4. Modulation strategy carriers disposition examples the for converters with (a) $N = 2$ and (b) $N = 3$. The carriers are displaced of $2\pi/N$ rad.

the definition in [37] that specifies an interphase transformer as "an electromagnetic device enabling the operation in parallel of two or more phase displaced commutating groups through inductive coupling between the windings placed on the same core," which is closely related to the definition in [38].

The basic implementation of a hypothetical MIPT T_k with N windings is shown in Fig. 3(a), where an N-limb core is employed. Since a symmetrical MIPT is not easily constructed for $N \geq 3$, other structures such as the whiffletree presented in [36] and seen in Fig. 3(b) are preferable for practical implementations. For the following analysis, the MIPTs will be considered as symmetric structures.

A. Converter Operation

The poles of the generic SPTT switches are connected to the respective windings at one end. By definition, a turned-on switch S_{kj} connects the transformer winding to the midpoint 0 of the dc-link. When the switch is turned OFF, the voltage on the pole is determined by the input current direction. Thus, the pole voltages across the switches, i.e., the voltages between each switch fixed terminal and the 0 terminal, are given by

$$v_{sk,j} = \text{sign}(i_k)\,\frac{V_o}{2}\,(1 - s_{kj}) \tag{3}$$

where the switching functions s_{kj} are defined as

$$s_{kj} = \begin{cases} 1, & \text{if switch } S_{kj} \text{ is ON} \\ 0, & \text{if switch } S_{kj} \text{ is OFF} \end{cases} \tag{4}$$

and the partial dc-link voltages are assumed balanced and constant, i.e., $v_{op} = v_{\text{on}} = V_o/2$.

Defining $N_{o,k}$ as the number of turned-off switches at phase k and $N_{c,k}$ as the number of turned-on switches at that phase, it follows that

$$N = N_{o,k} + N_{c,k}. \tag{5}$$

As presented in [18], according to the MIPT operation, the input phase voltages $v_{\text{in},k}$ generated by the converter are

$$v_{\text{in},k} = \frac{1}{N}\sum_{j=1}^{N} v_{sk,j} = \text{sign}(i_k)\,\frac{V_o N_{o,k}}{2N}. \tag{6}$$

From (4) and (6), the input phase voltages are rewritten as

$$v_{\text{in},k} = \text{sign}(i_k)\,\frac{V_o}{2}\left(1 - \frac{1}{N}\sum_{j=1}^{N} s_{kj}\right). \tag{7}$$

The input phase voltages, as defined in (7), present several levels depending on the switching signals, which are generated by the applied modulation strategy.

B. Multilevel Modulation Strategy

The modulation circuit of the presented converter has two elementary functions: to generate the desired input voltages $v_{\text{in},k}$ and guarantee the correct operation of the MIPTs, i.e., to avoid the saturation. Carrier-based PWM modulation variations are further considered in this study, even though more complex modulation schemes can be employed, e.g., space-vector modulation variations. This is to simplify the implementation in commercially available digital signal controller (DSC) devices assuming a large number of converter legs N.

The carrier-based modulation scheme employs a hybrid set of carriers as shown in Fig. 4. For even values of N, there are two in-phase disposition carrier subsets, where each subset is composed of N phase-shifted (PS) carriers displaced of $2\pi/N$ from each other. On the other hand, for an odd value of N, the two subsets of N PS carriers are in phase opposition disposition.

As there are two carriers per SPTT switch, the gate ON signal for a given switch S_{kj} occurs in two situations:

1) the modulation function m_k is lower than the respective carriers crr_{jp}, and m_k is positive;

2) the modulation function m_k is higher than the respective carriers crr_{jn}, and m_k is negative.

Thus, in each switching period T_s, all switches of the same phase operate with the same duty cycle d_k, but displaced by $2\pi/N$ rad, ensuring the appropriate MIPTs operation. Ideally, this type of operation leads to exclusively high-frequency voltage components across each MIPT winding and allows that these devices can have an optimized design with ferrite materials. On the other hand, this guarantees very low voltage steps across the boost inductors and these can be optimized for mainly wire losses with increased N.

As in other multilevel converters, such a modulation scheme leads to frequency multiplication on the input switched voltages. Herein, the first high-frequency harmonic group, i.e., the apparent frequency f_a is located around N times the switching frequency $f_s = 1/T_s$, which is an important feature to reduce input filter components.

III. PFC Rectifier Operation

The following analysis assumes ideal components, sinusoidal and balanced ac voltages, ripple-free input currents, and that the output voltages are constant and balanced.

The three-phase rectifier operation can be defined by modeling the ac side with

$$\vec{v}_{abc} = \mathbf{L}_{abc} \cdot \frac{d}{dt}\vec{i}_{abc} + \vec{v}_{\mathrm{in},abc} - \vec{v}_{Ne,0} \tag{8}$$

where

$$\vec{v}_{abc} = [v_a \ v_b \ v_c]^T \tag{9}$$

$$\vec{i}_{abc} = [i_a \ i_b \ i_c]^T \tag{10}$$

$$\vec{v}_{\mathrm{in},abc} = [v_{\mathrm{in},a} \ v_{\mathrm{in},b} \ v_{\mathrm{in},c}]^T \tag{11}$$

$$\mathbf{L}_{abc} = L_b \cdot \mathbf{I}_{3\times 3} \tag{12}$$

with $L_b = L_{b,a} = L_{b,b} = L_{b,c}$ and $\vec{v}_{Ne,0}$ being a column vector with the voltage between points Ne and 0 at its three components. The voltage component in $\vec{v}_{Ne,0}$ is also named here common mode (CM) voltage, v_{cm}, since the CM impedance of the MIPTs is null [18].

Assuming a purely sinusoidal mains voltage, the local average value of the voltages $v_{\mathrm{in},k}$ is required to be

$$\langle v_{in,k}\rangle = \sqrt{\hat{V}_g^2 + |V_{Lb}|^2}\cdot \sin\left(\omega_g t + \phi_k - \theta_{Lb}\right) \tag{13}$$

to achieve near unity power factor, where $|V_{Lb}| = \omega_g L_b \hat{I}$, $\theta_{Lb} = \arctan(|V_{Lb}|/\hat{V}_g)$, $\hat{I}$ is the peak current value of the sinusoidal input currents, and $\langle x\rangle$ denotes the local average value of variable x defined by

$$\langle x\rangle = \frac{1}{T_s}\int_{t-T_s}^{t} x\left(\tau\right)\ d\tau. \tag{14}$$

The values of $|V_{Lb}|$ and θ_{Lb} are typically very close to zero in practical implementations and will be neglected in the following analysis. Thus

$$\langle v_{\mathrm{in},k}\rangle \approx \hat{V}_g \cdot \sin\left(\omega_g t + \phi_k\right) \tag{15}$$

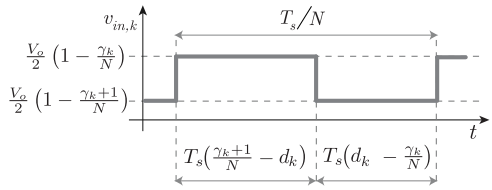

Fig. 5. Rectifier input voltage levels and respective time intervals in a general situation.

which should be generated by the modulation strategy that drives the converter. Therefore, neglecting the voltages across the boost inductors, for a high power factor operation and a sinusoidal grid voltage [cf., (1)], the local average values of the input voltages $\langle v_{\mathrm{in},k}\rangle$ must be

$$\begin{cases} \langle v_{\mathrm{in},a}\rangle = & M\frac{V_o}{2}\sin\left(\omega_g t\right) \\ \langle v_{\mathrm{in},b}\rangle = & M\frac{V_o}{2}\sin\left(\omega_g t - \frac{2\pi}{3}\right) \\ \langle v_{\mathrm{in},c}\rangle = & M\frac{V_o}{2}\sin\left(\omega_g t + \frac{2\pi}{3}\right) \end{cases} \tag{16}$$

where M is the modulation index given by

$$M = \frac{2\hat{V}_g}{V_o}. \tag{17}$$

The rectifier modulation functions are generated by the converter control system and then compared with the carriers to generate the gate signals. Considering the converter operation, from (16), the phase modulation functions are approximated with

$$\begin{cases} m_a &= M\sin\left(\omega_g t\right) \\ m_b &= M\sin\left(\omega_g t - \frac{2\pi}{3}\right) \\ m_c &= M\sin\left(\omega_g t + \frac{2\pi}{3}\right) \end{cases} \tag{18}$$

and in each phase k, the switches duty cycles are given by

$$d_k = 1 - M\left|\sin\left(\omega_g t + \phi_k\right)\right|. \tag{19}$$

Other modulation functions m_k lead to different characteristics and can be used as presented in [19]. Sinusoidal PWM is considered here for the sake of simplicity.

A. Multilevel Input Voltage Generation

From (7) and considering the time-variant duty cycle defined in (19), the input phase voltage varies between two well-defined levels at a given time interval. The levels depend on the operation ranges γ_k that are defined by

$$\gamma_k = \mathrm{floor}\left(N\cdot d_k\right). \tag{20}$$

The voltage levels and its time intervals are shown generically in Fig. 5. Note that the frequency at the input phase voltage $v_{\mathrm{in},k}$ is N times the semiconductor switching frequency $f_s = 1/T_s$. Furthermore, the voltage steps at the input phase voltage are $V_o/(2N)$.

Fig. 6 illustrates a three-phase MLMSR with $N = 2$ in a hypothetical condition with a modulation index $M = 0.86$ and

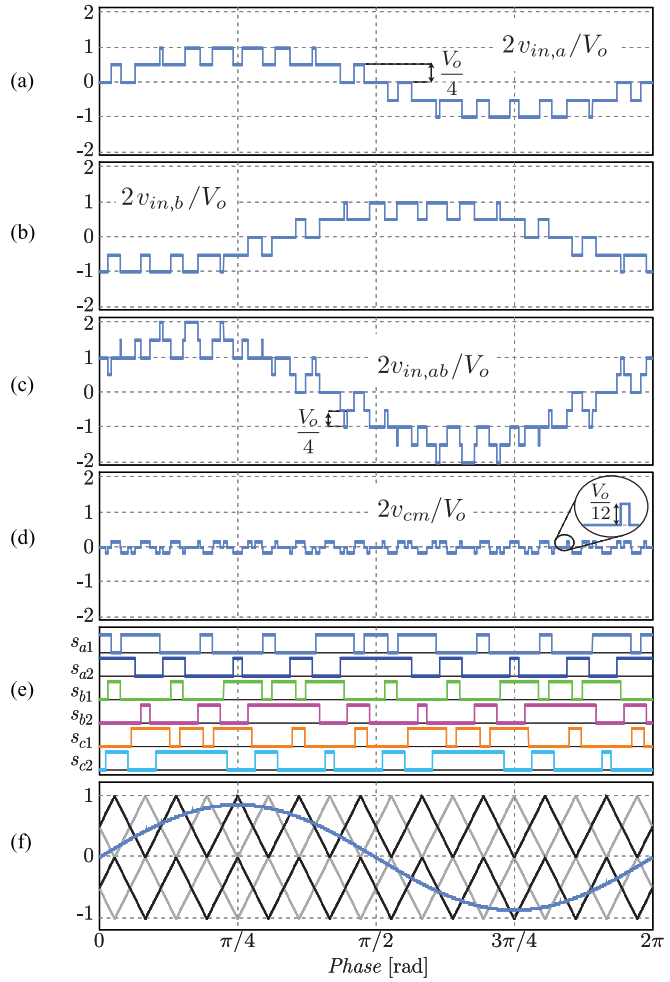

Fig. 6. Input voltage generation for an exemplary three-phase MLMSR with $N = 2$: (a) input phase voltage $v_{\mathrm{in},a}$; (b) input phase voltage $v_{\mathrm{in},b}$; (c) input line-to-line voltage $v_{\mathrm{in},ab}$; (d) CM voltage v_{cm}; (e) switching signals for all active switches; and (f) carriers and modulation signal m_a.

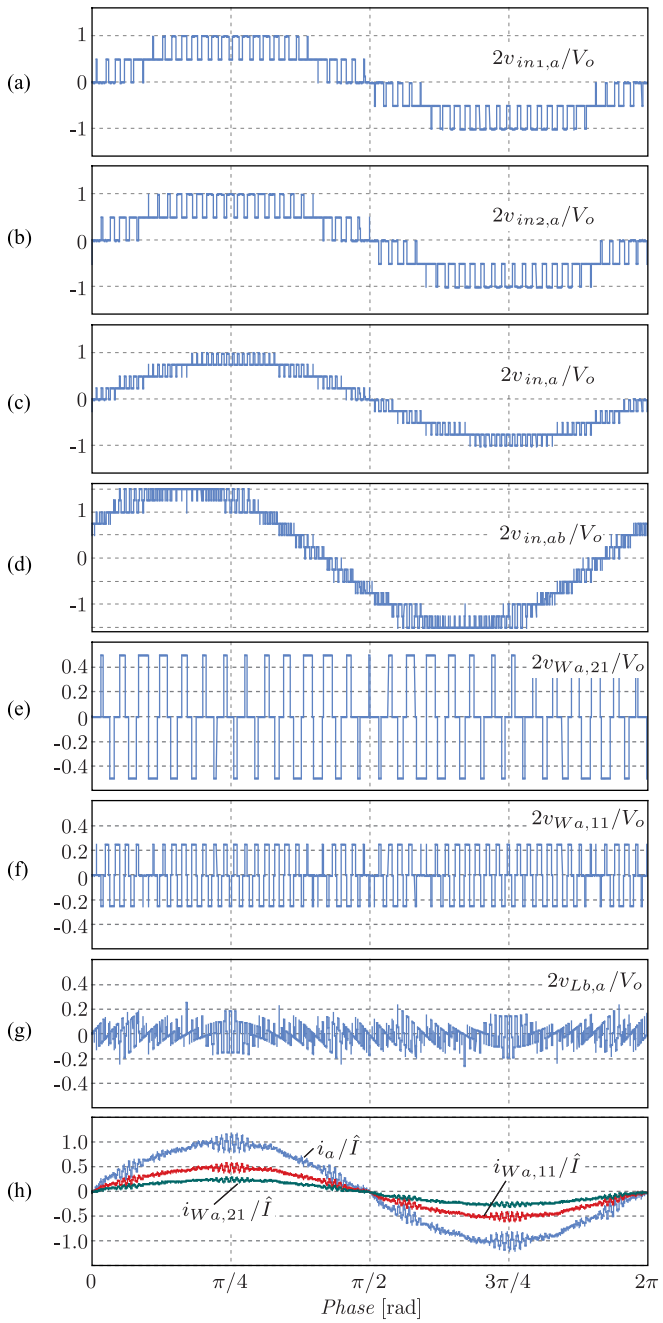

Fig. 7. Main waveforms of a rectifier with $N = 4$ (normalized): (a) $v_{\mathrm{in}1,a}$ (see Fig. 3); (b) $v_{\mathrm{in}2,a}$ (see Fig. 3); (c) input phase voltage $v_{\mathrm{in},a}$; (d) input line voltage $v_{\mathrm{in},ab}$; (e) winding $W_{a,21}$ voltage; (f) winding $W_{a,11}$ voltage; (g) voltage $v_{Lb,a}$ across the boost inductor; and (h) currents through the boost inductor and two of the MIPT windings.

$f_s = 9f_g$, where f_g is the fundamental grid frequency. The input phase voltages $v_{\mathrm{in},a}$ and $v_{\mathrm{in,b}}$ are shown in Fig. 6(a) and (b), respectively. The line-to-line input voltage $v_{\mathrm{in},ab}$ and the CM voltage $v_{\mathrm{cm}} = (v_{\mathrm{in},a} + v_{\mathrm{in},b} + v_{\mathrm{in},c})/3$ are shown in Fig. 6(c) and (d). All switch commands are presented in Fig. 6(e), and the modulation signal m_a and PWM carriers are shown in Fig. 6(f). The input voltages present five levels and the line-to-line voltage presents nine levels. The apparent frequency in the input voltages is, in this case ($N = 2$), two times the switching frequency. Furthermore, the converter exhibits a reduced CM voltage.

The main waveforms of a rectifier with $N = 4$ considering a whiffletree MIPTs configuration (see Fig. 3) are shown in Fig. 7 for a frequency ratio of $f_s/f_g = 27$ and a modulation index $M = 0.86$. The voltage in the nodes of the transformers are seen in Fig. 7(a)–(c), where the frequency multiplication effect is visible. Thirteen voltage levels are observed at the input line voltage waveform in Fig. 7(d). Fig. 7(e) and (f) shows the voltages across the windings of the transformers and the resulting boost inductor voltage is plotted in Fig. 7(g). Finally, the currents at the windings of the boost inductor and two of the MIPTs windings are in Fig. 7(h).

In order to provide a simple comparison, consider a conventional three-phase three-level unidirectional Vienna-type rectifier with the modulation strategy presented in [39], and the referred three-phase MLMSR with $N = 2$ employing the modulation scheme as shown in Fig. 4. In both cases, the frequency ratio is $f_s/f_g = 27$, and the modulation index is $M = 0.86$.

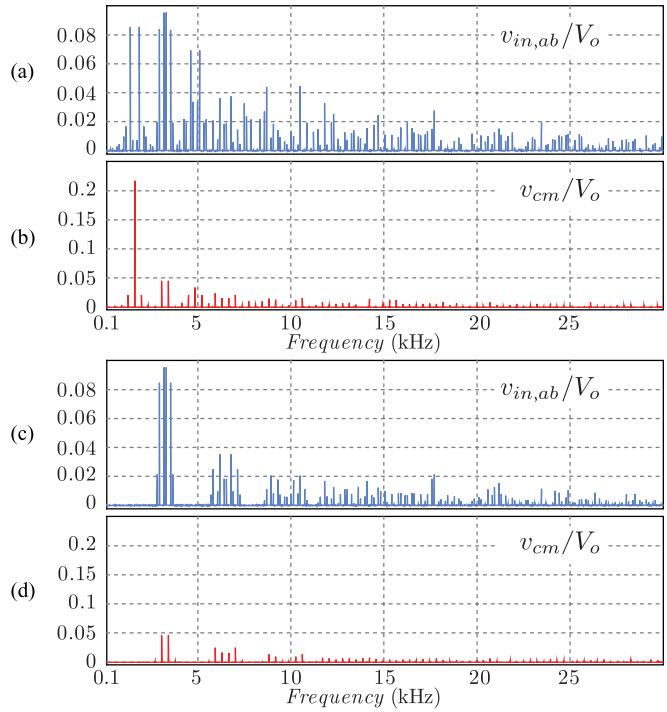

Fig. 8. Harmonic spectrum for (a) and (b) a three-phase three-level unidirectional Vienna-type rectifier and (c) and (d) three-phase MLMSR with $N = 2$ for a frequency ratio $f_s/f_g = 27$ and a modulation index $M = 0.86$. The results are normalized with respect to the output voltage V_o. The ideal cancellation of the low-order harmonics depends on the achieved command pulses symmetry and, in practice, depends on the control and modulation strategies.

Moreover, dc voltage sources on the output side and ac sinusoidal current sources on the input side are employed. The resultant harmonic spectra for the line-to-line input voltages $v_{\mathrm{in},ab}$ and for the CM voltage are shown in Fig. 8. Comparing with the conventional three-level converter [see Fig. 8(a) and (b)], it is seen that several harmonic groups are canceled in the MLMSR converter, as shown in Fig. 8(c) and (d).

B. Input Currents

Each phase boost inductor current i_k is found by solving the differential equation

$$L_{b,k}\frac{d}{dt}i_k = v_{Lb,k} = v_k - (v_{Wk,j} + v_{sk,j}) + v_{\mathrm{cm}} \tag{21}$$

where $v_{Wk,j}$ is the voltage across the winding W_{kj}. It can be proven that

$$v_{\mathrm{in},k} = v_{Wk,j} + v_{sk,j}. \tag{22}$$

The inductor voltages, v_{Lbk}, with $k = a, b, c$, are not uniquely determined by the respective input phase voltages, $v_{\mathrm{in},k}$, as it is the case for the single-phase rectifiers [26]. Thus, the input current ripple depends on the rectifier CM voltage v_{cm} and the input voltages $v_{\mathrm{in},k}$. Both are defined by the employed modulation strategy, number of semiconductor legs N, and modulation index M. Consequently, a general formulation for the input current ripple is a complex task. However, from (21) and (22) and considering the voltage levels and time intervals presented in Fig. 5, it is possible to obtain the high-frequency input current ripple Δi_{in} envelope.

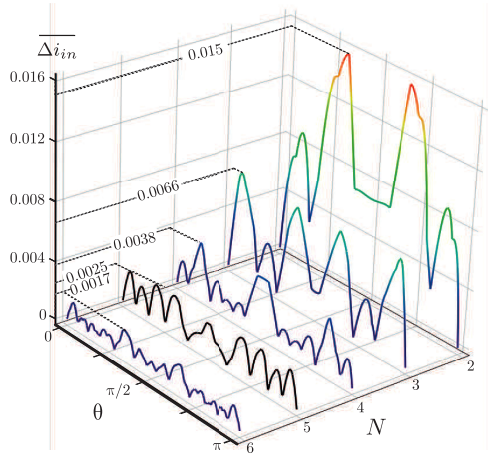

Fig. 9. Normalized phase "a" boost inductor current ripple envelope as a function of θ for converters with $N = 2.6$ and $M = 0.86$. The peak normalized ripple in a typical Vienna-type rectifier is $\overline{\Delta i_{\mathrm{in}}} \approx 0.028$ for the modulation scheme presented in [39].

Fig. 9 illustrates normalized input current envelopes $\overline{\Delta i_{\mathrm{in}}}$ as functions of the instantaneous input phase voltage angle θ for converters with $N = 2, 3, \ldots, 6$, operating with a modulation index $M = 0.86$. All results are normalized according to

$$\overline{\Delta i_{\mathrm{in}}} = \Delta i_{\mathrm{in}}\frac{f_s L_b}{V_o}. \tag{23}$$

The input current ripple is clearly reduced with increasing N and there are significant behavior changes with changing N. This result clarifies the benefits of the proposed converter regarding the input filters.

C. Multiinterphase Transformers Magnetizing Currents

According to (7), the generation of a given input phase voltage is related to the MIPT operation and the switching states. A simpler way to model the MIPT operation is to decompose the voltages and current across the windings into their local common and differential components [18]. It follows that the self- and mutual-inductances are uniquely represented through local CM and DM inductances. Each MIPT local CM inductance is null [18], while the DM ones are

$$L^{\mathrm{dm}}_{Wk,j} = L^{\mathrm{dm}}_{Wk} = \frac{N}{N-1}L_s \tag{24}$$

where L_s is the self-inductance of each winding. The local DM currents and voltages across the windings W_{kj} (with $j = 1, 2, \ldots, N$) are related according to

$$v^{\mathrm{dm}}_{Wk,j} = L^{\mathrm{dm}}_{Wk}\frac{d}{dt}i^{\mathrm{dm}}_{Wkj} \tag{25}$$

with

$$v^{\mathrm{dm}}_{Wk,j} = \mathrm{sign}(i_k)\frac{V_o(N-1)}{2N}\left(s_{kj} - \frac{1}{N}\sum_{j=1}^{N} s_{kj}\right). \tag{26}$$

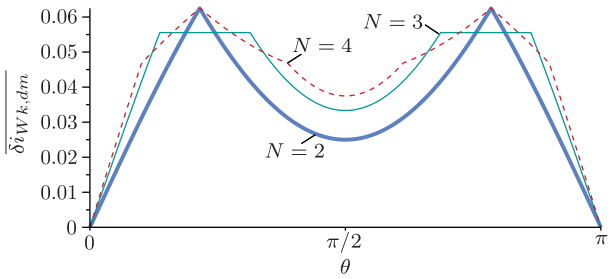

Fig. 10. Normalized local differential mode current (magnetizing current) envelope of the MIPT windings.

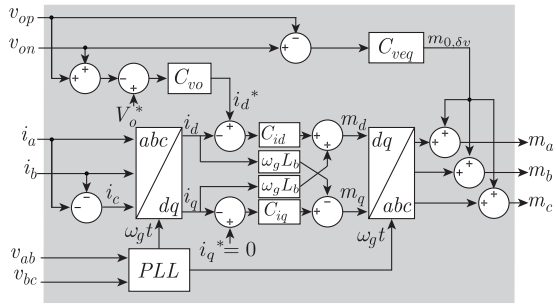

Fig. 11. Block diagram of the used control strategy.

The DM inductances L_{Wk}^{dm} are responsible for limiting the interphase circulating currents, i.e., the local DM or magnetizing currents of an MIPT. Such currents influence the losses and the general operation of the converter, since high DM currents lead to early discontinuous conduction mode operation. Thus, the magnitude of the DM currents must be evaluated.

From (25), (26), and Fig. 5, the envelope of the DM currents across the windings is obtained from the integration of the DM voltage, resulting in

$$\delta i_{Wk}^{\mathrm{dm}} = \frac{V_o}{4Nf_s L_W^{\mathrm{dm}}} \left[d_k \left(-2\gamma_k - 1 + N \right) + \frac{\gamma_k \left(\gamma_k + 1 \right)}{N} \right]. \tag{27}$$

Defining the normalized DM current envelope as

$$\overline{\delta i_{Wk}^{\mathrm{dm}}} = \delta i_{Wk}^{\mathrm{dm}} \frac{L_W^{\mathrm{dm}} f_s}{V_o} \tag{28}$$

the positive DM current envelope is presented in Fig. 10, for different values of N and $0 < \theta < \pi$, considering the modulation strategy introduced in Section II-B with a modulation index of $M = 0.8$. Equation (28) can be used to define the value of the required magnetizing inductance. The leakage inductance in these transformers can be used to reduce the current ripple at the boost inductor and, thus, do not affect the operation of the converter in a relevant way. However, an air gap will influence the winding losses and reduce the total magnetizing inductance. Its presence can reduce the possibility of saturation due to low-frequency flux harmonics generated by small deviations of the duration of the gate pulses. Therefore, the magnetizing flux and the winding currents are the main design parameters to be considered.

It should be observed that the magnetizing current is directly related to the magnetic flux in the transformers. In this sense, its behavior should be evaluated, since the total losses and volume of a transformer depend on its magnetic flux density. Furthermore, a modulation strategy must guarantee that the local average value of all MIPTs magnetizing currents, and implicitly the magnetic flux in their cores, in each switching period is null. Thus, the modulation strategy must achieve

$$\langle i_{Wkj,\mathrm{dm}} \rangle = 0 \tag{29}$$

in each switching period for the optimal design of the MIPTs.

D. PFC-Oriented Control Strategy

Even though the proposed topology presents multilevel and frequency multiplication at the input voltages and output currents, from the control point of view, the MLMSR converter is very similar to the conventional unidirectional three-phase three-level rectifier. This occurs because, ideally, the MIPTs do not present CM inductance and, thus, do not influence the input current dynamics. However, the MIPT must be designed for a high differential inductance, i.e., for a high rate of CM/DM currents in the transformer windings, in order to avoid discontinuous operation, which occurs when the diodes D_{jkp} and D_{jkn} turn-off prematurely.

Among various control schemes, a synchronous reference frame strategy is used in this study. It is implemented as shown in Fig. 11. This control scheme includes an output voltage balancing loop and has been presented for unidirectional three-phase three-level unidirectional rectifiers in works such as [40] and [41] with small modifications.

The instantaneous phase angle $\omega_g t$ is obtained from the grid line-to-line voltage measurements v_{ab} and v_{bc} by means of a phase-locked loop circuit. The total output voltage V_o control loop generates the direct axis current reference $i_d{}^*$, and the quadrature axis current reference is set to zero. The measured input currents i_a and i_b are converted to the synchronous reference system through the abc/dq transformation and are directly controlled in dq variables. Finally, the modulation signals m_k are obtained from a dq/abc transformation of the control signals m_d and m_q, as well as the output control signal $m_{0,\delta v}$, generated from the partial output voltage balance loop.

It should be noted that the frequency multiplication and multilevel operation allows a converter design with a reduced value of inductance at the $L_{b,k}$ inductors. However, the crossover frequency of the current control loop will not be necessarily higher, in comparison with other conventional rectifiers, since the transformer operates at the switching frequency. Therefore, the digital modulation circuit must be updated at this frequency in order to guarantee the adequate operation without magnetic saturation. Besides, other issues such as digital control delays typically limit the dynamics of the current control. On the other hand, the reduced inductance value of $L_{b,k}$ makes the system more susceptible to disturbances mainly to the grid voltage, which typically presents harmonic distortion and unbalance. In such situations, simple controllers such as PI and PID may be

inefficient and more complex control structures such as multiple resonant controllers may be necessary, mainly for these periodic disturbances.

IV. Practical Implementation for the SPTT Switch and Current Efforts

The SPTT switch in the converter of Fig. 1 can be implemented through different semiconductor configurations. In this study, six examples are considered (cf., Fig. 2) including some variations. Such configurations differ regarding the number of controlled devices, gate drivers, and the requirements regarding the isolated auxiliary power supplies, voltage and current efforts, complexity of the modulation circuits, among other issues. However, all cases generate the same external converter characteristics for PFC operation as previously discussed.

According to the application requirements, both IGBTs, MOSFETs, or other power semiconductor devices can be chosen for the turn-off devices. For high power density applications, MOSFETS are typically preferred. In high-power applications, where high-current devices are necessary, IGBTs are typically used. Moreover, several other recent and emerging semiconductor technologies such as SiC-JFETS, SiC-MOSFETS, and GaN devices [11], [12] are promising devices for current and future MLMSR applications.

As seen in Fig. 2(b), configuration I [3] requires two driver circuits with insulated references. On the other hand, the controlled devices S_1 and S_2 are easily driven by the same gate signal and diodes D_1 and D_2 operate at the grid frequency.

Configuration II [cf., Fig. 2(c)] [27] needs two isolated gate drivers and allows simpler modulation circuits, as with configuration I. However, a more complex modulation circuit might bring benefits if MOSFETs are used, where a synchronous modulation scheme can be implemented in order to reduce the conduction losses. Thus, for the positive half cycle, switch S_2 is driven with the control gate signal, while S_1 is continuously ON, reducing the conduction losses in D_1/S_1. Complementary operation occurs in the negative half cycle.

A potentially inexpensive solution is presented in Fig. 2(d) [4], where a single turn-off device and its gate drive are required. The main drawback is the increased conduction losses, since there are three devices carrying current in one of the operation states.

Configuration IV [cf., Fig. 2(e)] consists of a T-type arrangement [28]. The central bidirectional switch may be realized in different ways, as shown in Fig. 2(h)–(j) [4], [30]. This scheme reduces the number of devices in the current path when the switches are OFF. However, in this case, the external diodes D_{kjp} and D_{kjn} must be rated for the full dc-link voltage V_o.

A general switch implementation is presented in Fig. 2(f) [25] and allows many variations. For instance, all semiconductors may be synchronously commanded, sharing the current efforts. Furthermore, it is possible to switch ON the MOSFETs related to the diodes that conduct in the complementary time $(1-d)T_s$ and, thus, reduce the forward voltage drop across such devices. The main disadvantage is the requirement for four gate drive circuits and consequently higher implementation cost. Another possibility is to employ exclusively the MOSFETs S_2 and S_4, which share the same reference, reducing the auxiliary power supply requirements.

Fig. 2(g) shows configuration VI, in which a bidirectional switch [such as the ones shown in Fig. 2(h)–(j)] is placed in between the pole and the 0 terminal. This leads to reduced conduction losses since the current is divided into two paths. Nevertheless, such a scheme requires two additional gate circuits and their respective auxiliary power supplies.

Table I summarizes the current efforts for all devices of configurations I–IV and for the diodes D_{kjp} and D_{kjn}. The efforts for the other cases are not included, since these depend on the employed modulation scheme and mainly of the static characteristics of considered devices, and thus, cannot be generalized.

TABLE I
Semiconductor Efforts for the SPTT Switches Configurations I, II, III, and IV Presented in Fig. 2, and for the Diodes D_{kjp} and $D_{kjn}(k=a,b,c)$

SPTT Model	Device	I_{avg}	I_{rms}
I	$D_1\ D_2$	$\frac{\hat{I}_{in}}{\pi N}$	$\frac{\hat{I}_{in}}{2N}$
	$S_1\ S_2$	$\frac{\hat{I}_{in}}{4\pi N}(4-M\pi)$	$\frac{\hat{I}_{in}}{N}\sqrt{\frac{1}{4}-\frac{2M}{3\pi}}$
II	$D_1\ D_2$	$\frac{\hat{I}_{in}M}{4N}$	$\frac{\hat{I}_{in}}{N}\sqrt{\frac{2M}{3\pi}}$
	$S_1\ S_2\ D_3\ D_4$	$\frac{\hat{I}_{in}}{4\pi N}(4-M\pi)$	$\frac{\hat{I}_{in}}{N}\sqrt{\frac{1}{4}-\frac{2M}{3\pi}}$
III	$D_1\ D_2$	$\frac{\hat{I}_{in}}{\pi N}$	$\frac{\hat{I}_{in}}{2N}$
	$D_3\ D_4$	$\frac{\hat{I}_{in}}{4\pi N}(4-M\pi)$	$\frac{\hat{I}_{in}}{N}\sqrt{\frac{1}{4}-\frac{2M}{3\pi}}$
	S_1	$\frac{\hat{I}_{in}}{2\pi N}(4-M\pi)$	$\frac{\hat{I}_{in}}{N}\sqrt{\frac{1}{2}-\frac{4M}{3\pi}}$
IV(h)	$D_5\ D_6\ D_7\ D_8$	$\frac{\hat{I}_{in}}{4\pi N}(4-M\pi)$	$\frac{\hat{I}_{in}}{N}\sqrt{\frac{1}{4}-\frac{2M}{3\pi}}$
	S_5	$\frac{\hat{I}_{in}}{2\pi N}(4-M\pi)$	$\frac{\hat{I}_{in}}{N}\sqrt{\frac{1}{2}-\frac{4M}{3\pi}}$
IV(i)	$D_9\ D_{10}\ S_6\ S_7$	$\frac{\hat{I}_{in}}{4\pi N}(4-M\pi)$	$\frac{\hat{I}_{in}}{N}\sqrt{\frac{1}{4}-\frac{2M}{3\pi}}$
IV(j)	$D_{11}\ D_{12}\ S_8\ S_9$	$\frac{\hat{I}_{in}}{4\pi N}(4-M\pi)$	$\frac{\hat{I}_{in}}{N}\sqrt{\frac{1}{4}-\frac{2M}{3\pi}}$
All	$D_{kjp}\ D_{kjn}$	$\frac{\hat{I}_{in}M}{4N}$	$\frac{\hat{I}_{in}}{N}\sqrt{\frac{2M}{3\pi}}$

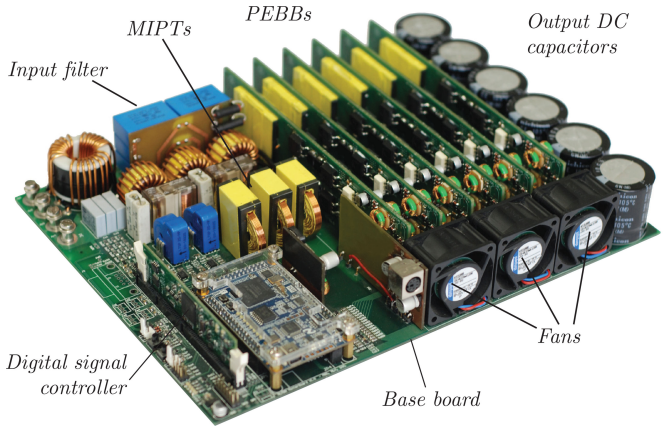

Fig. 12. Built 7.5-kW three-phase MLMSR modular prototype with $N=4$.

V. Experimental Results

A three-phase MLMSR laboratory prototype (cf., Fig. 12) with $N=4$ has been built based on a modular construction

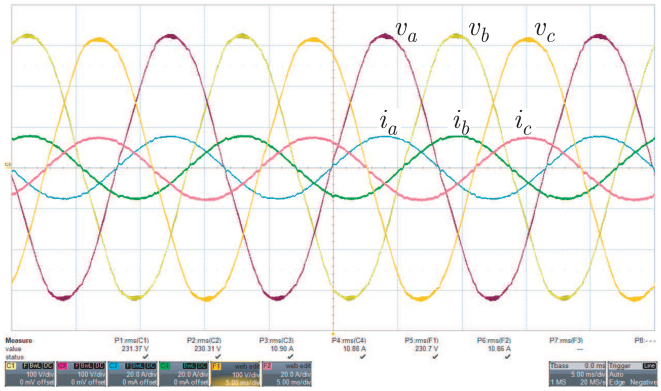

Fig. 13. Experimental results: grid phase voltages v_k (100 V/div) and grid currents i_k (20 A/div). The converter presents low-current total harmonic distortion THD$i = 1.82\%$ and high power factor PF > 0.99.

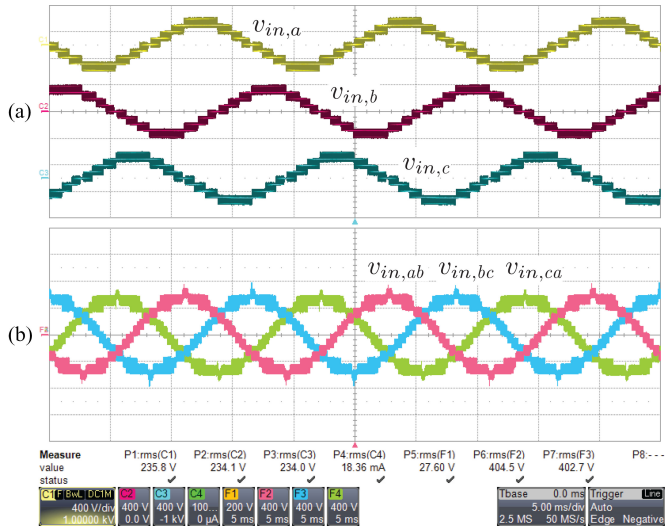

Fig. 14. Experimental results: (a) input phase voltages $v_{\mathrm{in},k}$ (400 V/div) and (b) input line-to-line voltages (400 V/div).

architecture [42] using the switching network of Fig. 2(b) and the whiffletree configuration shown in Fig. 3. The converter operates at the switching frequency $f_s = 75\,\mathrm{kHz}$, with the following specifications: rated output power $P_o = 7.5\,\mathrm{kW}$, output voltage $V_o = 760\,\mathrm{V}$, and input phase rms voltage $v_k = 230\,\mathrm{V}/60\,\mathrm{Hz}$. All control and modulation schemes are implemented within a DSC TMS320F28335 (Texas Instruments).

The grid phase voltages and currents are shown in Fig. 13, where high power factor and low-current harmonic distortion are obtained.

As shown in Fig. 14, the input phase voltages $v_{\mathrm{in},k}$ present nine levels and there are 13 line-to-line voltage levels.

Besides frequency multiplication provided by the modulation scheme ($f_a = Nf_s = 300\,\mathrm{kHz}$), the multilevel operation reduces the voltage steps across the boost inductors $L_{b,k}$, and thus, low-current ripple is obtained. This is seen in Fig. 15, where the voltage and the current in a boost inductor are shown.

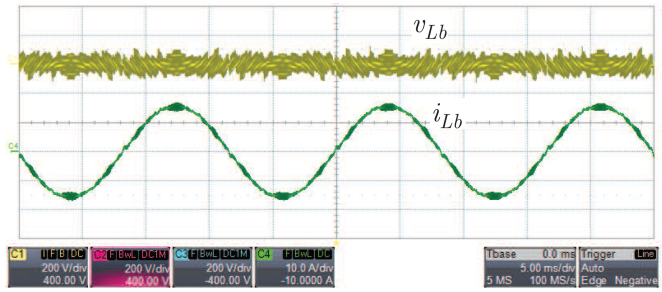

Fig. 15. Experimental waveforms of the voltage v_{Lb} (200 V/div) and current i_{Lb} (10 A/div) across the boost inductor $L_{b,a}$.

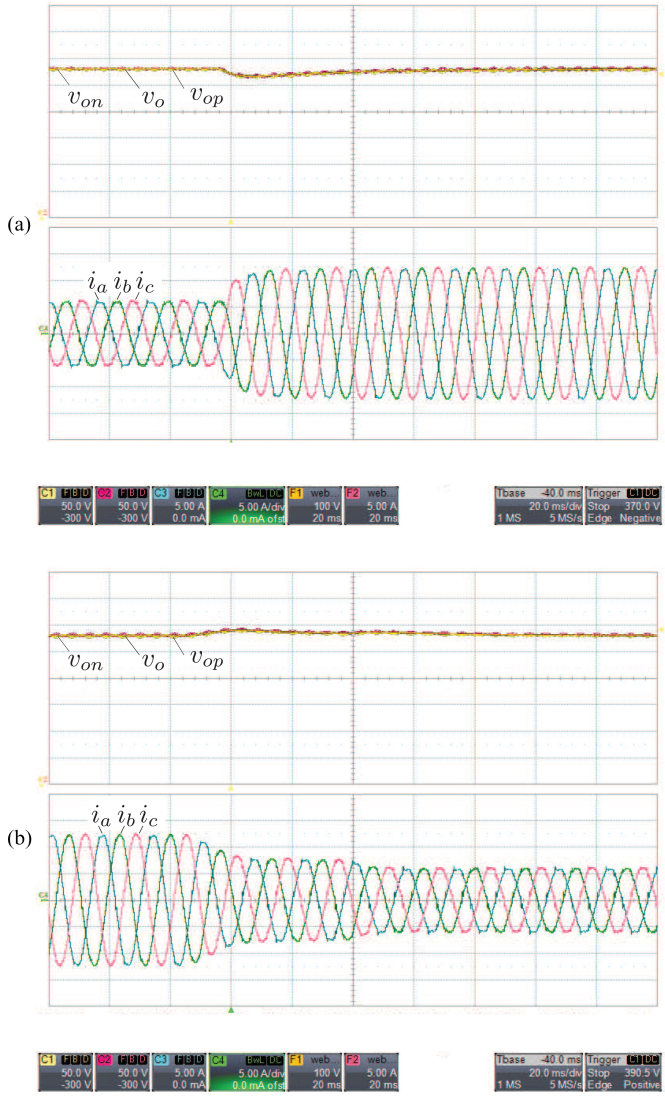

Fig. 16. Experimental waveforms of the partial dc-link voltages v_{op} and v_{on} (50 V/div), total output voltage v_o (100 V/div) and grid currents i_k (5 A/div) during load transients. (a) Positive step load (40–80%) and (b) a negative step load (80–40%).

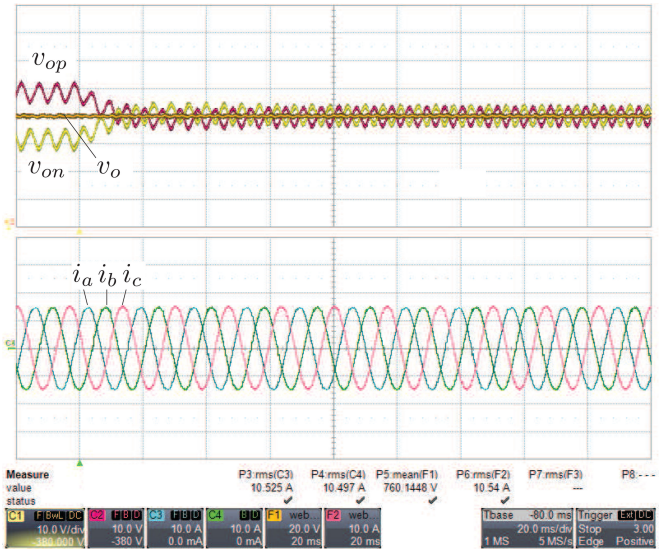

Fig. 17. Partial dc-link voltages v_{op} and $v_{\rm on}$ (10 V/div), total output voltage v_o (20 V/div) and grid currents i_k (10 A/div) showing the dc-link voltages balancing control loop operation. The closed-loop operation starts at $t = -80\,\rm ms$.

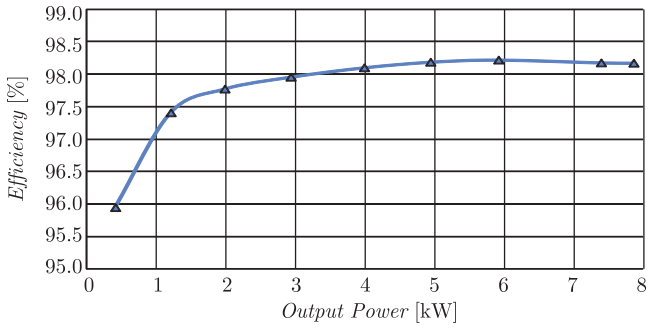

Fig. 18. Measured efficiency as a function of the output power with rated grid phase voltage, i.e., $v_k^{\rm rms} = 230\,\rm V$. The auxiliary power supply for gate drivers, fans, and control has not been considered.

A fast transient response is observed in Fig. 16(a), when a positive load step (40–80%) occurs. Similarly, the converter exhibits fast response and low overshoot for a negative load step (80–40%), as shown in Fig. 16(b). In both cases, the input currents present a smooth behavior during the transient events.

The output voltage balance control action is observed in Fig. 17. Initially, a small load difference makes the output voltages have different values and the balance control is inactive. At $t = -80\,\rm ms$, the balance is activated and the partial output voltages are rapidly balanced. The total output voltage remains regulated before, during, and after the transient event.

As shown in Fig. 18, the converter presents a flat efficiency curve over a wide load power range. Furthermore, it is seen that the converter efficiency is above 98% for output power higher than 3.5 kW.

Finally, the grid current harmonic spectrum and the IEC 61000-3-2 class A limits are presented in Fig. 19. The

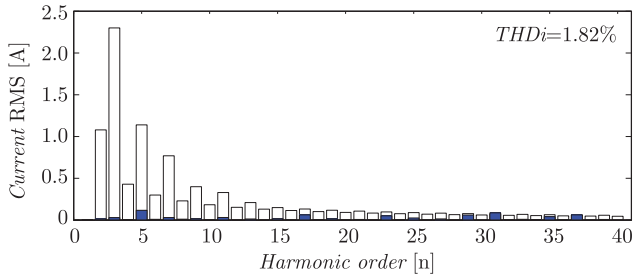

Fig. 19. Grid current harmonic spectrum and IEC 61000-3-2 class A limits for the MLMSR operation at rated power.

converter presents low total harmonic distortion with a current total harmonic distortion of THD$i \approx 1.82\%$ at rated power.

VI. Conclusion

The three-phase PFC multilevel rectifier employing multistate switching cells has been presented, including appropriate operation, modulation, and control strategies. Two solutions were discussed for the implementation of the MIPTs, where a whiffletree configuration is shown as a promising alternative for a high number of switching networks per phase leg and a conventional multilimb core is suitable up to three legs. The ripple current envelopes for the boost inductor and the magnetizing inductances of the MIPTs were derived and can be used to design these components. Alternatives to the switching networks configuration were discussed on the basis of a comparison between various SPTT switch possibilities including practical implementation aspects, such as the number of required isolated gate drivers and the possibility of using synchronous rectification techniques, added to the current efforts computation expressions for the main power semiconductors. Experimental results from a four legs per phase lab prototype were presented, where efficiency levels above 98% from 40% load and IEC61000-3-2 class A requirements regarding mains current distortion were observed.

Despite the increased control/modulation complexity and number of devices, the presented concept can be an attractive alternative to high-power three-phase rectification with low impact in the mains due to its modular structure that enables the separate design optimization of the magnetic components, e.g., boost inductors built with iron powder materials and MIPTs with ferrite cores; the use of reduced ratings power semiconductor devices with very low switching losses; the effective parallelism of these devices to reduce conduction losses; the benefits of modularization for manufacturing process and reliability; the overall converter size/weight reduction including those of the cooling systems; the reduction of filter elements due to the reduced magnitude of the voltage steps applied at the input of the converter and reduced currents at the dc-link; and the possibility of integration for high-power converters.

REFERENCES

[1] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 641–660, Jun. 2004.

[2] J. Kolar and T. Friedli, "The essence of three-phase PFC rectifier systems—Part I," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 176–198, Jan. 2013.

[3] Y. Zhao, Y. Li, and T. A. Lipo, "Force commutated three level boost type rectifier," in *Proc. IEEE Conf. Rec. Ind. Appl. Soc. Annu. Meet.*, 1993, vol. 2, pp. 771–777.

[4] J. W. Kolar and F. C. Zach, "A novel three-phase utility interface minimizing line current harmonics of high-power telecommunications rectifier modules," *IEEE Trans. Ind. Electron.*, vol. 44, no. 4, pp. 456–467, Aug. 1997.

[5] T. Friedli, M. Hartmann, and J. Kolar, "The essence of three-phase PFC rectifier systems—Part II," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 543–560, Feb. 2014.

[6] X. She, A. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013.

[7] D. Boroyevich, I. Cvetkovic, R. Burgos, and D. Dong, "Intergrid: A future electronic energy network?" *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 127–138, Sep. 2013.

[8] B. Bose, "Power electronics and motor drives recent progress and perspective," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 581–588, Feb. 2009.

[9] J. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance trends and limitations of power electronic systems," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst.*, 2010, pp. 1–20.

[10] J. Kassakian and T. Jahns, "Evolving and emerging applications of power electronics in systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 2, pp. 47–58, Jun. 2013.

[11] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[12] R. Mitova, R. Ghosh, U. Mhaskar, D. Klikic, M.-X. Wang, and A. Dentella, "Investigations of 600-v GaN HEMT and GaN diode for power converter applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2441–2452, May 2014.

[13] J. D. Van Wyk and F. Lee, "On a future for power electronics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 2, pp. 59–72, Jun. 2013.

[14] G. Torrico-Bascope and I. Barbi, "A single phase PFC 3 kW converter using a three-state switching cell," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, 2004, vol. 5, pp. 4037–4042.

[15] M. L. Heldwein and I. Barbi, "Boost-type unidirectional multilevel converters based on the connection of multiple converters through multi-state switching cells (in Portuguese)," Brazil Patent PI0 805 177, 2008.

[16] F. Heerdt, Z. Wu, L. Luo, and Y. You, "A multi-state switch and a converter employing the multi-state switch (in Chinese)," World Patent 2 009 106 014, 2009.

[17] G. V. Torrico-Bascope, "Method and device of electrical power," U.S. Patent 8 395 913, 2011.

[18] M. S. Ortmann, S. A. Mussa, and M. L. Heldwein, "Generalized analysis of a multistate switching cells-based single-phase multilevel PFC rectifier," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 46–56, Jan. 2012.

[19] M. S. Ortmann, S. A. Mussa, and M. L. Heldwein, "Evaluation of carrier-based PWM strategies for multi-state switching cells-based multilevel three-phase rectifiers," in *Proc. Braz. Power Electron. Conf.*, 2011, pp. 903–910.

[20] R. da Camara, P. Praca, C. M. T. Cruz, R. Torrico-Bascope, C. E. A. Silva, D. Oliveira, and L. H. S. C. Barreto, "Three-phase voltage doubler rectifier based on three-state switching cell for uninterruptible power supply applications using fpga," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 837–843.

[21] D. Floricau and V. Pangratie, "New unidirectional five-level VIENNA rectifier for high-current applications," in *Proc. IEEE 39th Annu. Conf. Ind. Electron. Soc.*, 2013, pp. 1080–1085.

[22] *Flatpack 2 48v he rectifiers datasheet*, Eltek, Drammen, Norway, 2012.

[23] *Large Capacity Power System tp483000d Datasheet*, Huawei Industrial Base, Shenzhen, China, 2013.

[24] *Electromagnetic Compatibility (EMC)—Part 3-2: Limits—Limits for Harmonic Current Emissions (Equipment Input Current ≤16 a Per Phase)*, IEC 61000-3-2-1 ed 3.2, 2009.

[25] M. S. Ortmann, S. A. Mussa, and M. L. Heldwein, "Concepts for high efficiency single-phase three-level PWM rectifiers," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 3768–3775.

[26] M. S. Ortmann, S. A. Mussa, and M. L. Heldwein, "Theoretical analysis of a single-phase three-level PFC converter employing multi-state switching cells," in *Proc. Braz. Power Electron. Conf.*, 2009, pp. 1185–1192.

[27] K. Corzine and J. Baker, "Reduced-parts-count multilevel rectifiers," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 766–774, Aug. 2002.

[28] K. Oguchi and Y. Maki, "Proposal of a multilevel-voltage source type rectifier having a three-phase diode bridge circuit as a main power circuit," (in Japanese), *IEEE J. Trans. Ind. Appl.*, vol. 112, no. 6, pp. 579–580, 1992.

[29] L. Parvulescu, D. Floricau, and M. Covrig, "Comparison between three level rectifiers," *U.P.B. Sci. Bull., Series C*, vol. 73, no. 2, pp. 295–304, 2011.

[30] R. Gules, A. Martins, and I. Barbi, "A switched-mode three-phase three-level telecommunications rectifier," presented at the 21st Int. Telecommun. Energy Conf., Copenhagen, Denmark, 1999.

[31] B. Cougo, T. Meynard, and G. Gateau, "Parallel three-phase inverters: Optimal PWM method for flux reduction in intercell transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug. 2011.

[32] B. Cougo, T. Friedli, D. Boillat, and J. Kolar, "Comparative evaluation of individual and coupled inductor arrangements for input filters of PV inverter systems," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst.*, 2012, pp. 1–8.

[33] P.-W. Lee, Y. S. Lee, D.-W. Cheng, and X.-C. Liu, "Steady-state analysis of an interleaved boost converter with coupled inductors," *IEEE Trans. Ind. Electron.*, vol. 47, no. 4, pp. 787–795, Aug. 2000.

[34] M. Hirakawa, Y. Watanabe, M. Nagano, K. Andoh, S. Nakatomi, S. Hashino, and T. Shimizu, "High power dc/dc converter using extreme close-coupled inductors aimed for electric vehicles," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 2941–2948.

[35] F. Ueda, K. Matsui, M. Asao, and K. Tsuboi, "Parallel-connections of pulsewidth modulated inverters using current sharing reactors," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 673–679, Nov. 1995.

[36] P. In Gyu and K. Seon Ik, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Proc. 28th IEEE Annu. Power Electron. Spec. Conf.*, 1997, vol. 2, pp. 1164–1170.

[37] *Converter Transformers—Part 1: Transformers for Industrial Applications*, IEC 61378-1 ed 2.0, 2011.

[38] *IEEE Standard Terminology for Power and Distribution Transformers*, IEEE Std C57.12.80-2002 (Revision of IEEE Std C57.12.80-1978), 2002.

[39] N. Backman and R. Rojas, "Modern circuit topology enables compact power factor corrected three-phase rectifier module," in *Proc. 24th Annu. Int. Telecommun. Energy Conf.*, 2002, pp. 107–114.

[40] L. Rixin, W. Fei, R. Burgos, D. Boroyevich, J. Dong, and Z. Di, "Average modeling and control design for VIENNA-type rectifiers considering the dc-link voltage balance," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2509–2522, Nov. 2009.

[41] M. L. Heldwein, S. A. Mussa, and I. Barbi, "Three-phase multilevel PWM rectifiers based on conventional bidirectional converters," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 545–549, Mar. 2010.

[42] M. S. Ortmann, W. Hoffmann, S. A. Mussa, and M. L. Heldwein, "Multilevel multistate switching cells PEBBs as the basis for the implementation of advanced rectifiers," in *Proc. IEEE 28th Annu. Appl. Power Electron. Conf. Expo.*, 2013, pp. 1871–1877.

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